

9. (Amended) A method of forming a gate oxide on a transistor body region, comprising:
evaporation depositing a metal layer on the body region using a substantially thermal process, the metal being chosen from the group IVB elements of the periodic table; and
oxidizing the metal layer using a krypton(Kr)/oxygen (O₂) mixed plasma process to form a metal oxide layer on the body region.
14. (Amended) A method of forming a transistor, comprising:
forming first and second source/drain regions;
forming a body region between the first and second source/drain regions;
evaporation depositing a metal layer on the body region using a substantially thermal process, the metal being chosen from the group IVB elements of the periodic table;
oxidizing the metal layer to form a metal oxide layer on the body region; and
coupling a gate to the metal oxide layer.
22. (Amended) A method of forming a memory array, comprising:
forming a number of access transistors, comprising:
forming first and second source/drain regions;
forming a body region between the first and second source/drain regions;
evaporation depositing a metal layer on the body region using a substantially thermal process, the metal being chosen from the group IVB elements of the periodic table;
oxidizing the metal layer to form a metal oxide layer on the body region;
coupling a gate to the metal oxide layer;
forming a number of wordlines coupled to a number of the gates of the number of access transistors;
forming a number of sourcelines coupled to a number of the first source/drain regions of the number of access transistors; and
forming a number of bitlines coupled to a number of the second source/drain regions of the number of access transistors.

30. (Amended) A method of forming an information handling system, comprising:
- forming a processor;
 - forming a memory array, comprising:
 - forming a number of access transistors, comprising:
 - forming first and second source/drain regions;
 - forming a body region between the first and second source/drain regions;
 - evaporation depositing a metal layer on the body region using a substantially thermal process, the metal being chosen from the group IVB elements of the periodic table;
 - oxidizing the metal layer to form a metal oxide layer on the body region;
 - coupling a gate to the metal oxide layer;
 - forming a number of wordlines coupled to a number of the gates of the number of access transistors;
 - forming a number of sourcelines coupled to a number of the first source/drain regions of the number of access transistors;
 - forming a number of bitlines coupled to a number of the second source/drain regions of the number of access transistors; and
 - forming a system bus that couples the processor to the memory array.
51. (Amended) A transistor formed by the process, comprising:
- forming a body region coupled between a first source/drain region and a second source/drain region;
 - evaporation depositing a metal layer on the body region using a substantially thermal process, the metal being chosen from the group IVB elements of the periodic table;
 - oxidizing the metal layer to form a metal oxide layer on the body region; and
 - coupling a gate to the metal oxide layer.